2005 IEEE International Symposium on Circuits and Systems (ISCAS)

Kobe, Japan
May 23-26, 2005

Volume 2 of 6
A3L-M  Audio & Speech Enhancement II (Lecture)
Time:    Tuesday, May 24, 2005, 14:00 - 16:00
Place:   Room 504
Co-Chairs: Masahide Abe, Tohoku University
          Heping Ding, National Research Council, Canada

14:00
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14:20
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Takeo Yasuda, IBM Japan

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Chair: Radu M. Secareanu, Arizona State University

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**Chair:** Bassel Soudan, *University of Sharjah*

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Place:  Reception Hall - Area 5
Chair:  Bah Hwee Gwee, Nanyang Technological University

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Time: Tuesday, May 24, 2005, 14:00 - 16:00
Place: Reception Hall - Area 6
Chair: U. B. Desai, ITT-Bombay

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Saed Samadi, M. Omair Ahmad, M.N.S. Swamy, Concordia University, Canada
Communications Circuit Design (Poster)

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A3P-Y.8 AN HIGH SPEED INTEGRATED EQUALIZER FOR DISPERSION COMPENSATION IN 10GB/S FIBER NETWORKS
Vasanth Kakani, Foster F. Dai, Richard C. Jaeger, Auburn University, USA
A4L-A SPECIAL SESSION - ESD Protection Design for Nanoelectronics & Gigascale Systems (Lecture)

Time: Tuesday, May 24, 2005, 16:10 - 18:10
Place: Room 301
Chair: Ming-Dou Ker, National Chiao Tung University

16:10
A4L-A.1 ESD PROTECTION DESIGN FOR I/O CELLS IN SUB-130-NM CMOS TECHNOLOGY WITH EMBEDDED SCR STRUCTURE
Kun-Hsien Lin, Industrial Technology Research Institute, Taiwan ROC; Ming-Dou Ker, National Chiao Tung University, Taiwan ROC

16:30
A4L-A.3 A NOVEL SUBSTRATE-TRIGGERED ESD PROTECTION STRUCTURE FOR A BUS SWITCH IC WITH ON-CHIP SUBSTRATE-PUMP
Paul C. F. Tong, Ping-Ping Xu, Wensong Chen, John Hui, Patty Z.Q. Liu, Pericom Semiconductor Corp, USA

16:50
A4L-A.4 ESD PROTECTION CIRCUIT DESIGN FOR ULTRA-SENSITIVE I/O APPLICATIONS IN ADVANCED SUB-90NM CMOS TECHNOLOGIES
Markus Mergens, Infineon Technologies AG, Germany; Geert Wybo, Benjamin Van Camp, Bart Keppens, Frederic De Ranter, Koen Verhaege, Phil Jozwiak, John Armer, Sarnoff Europe, Belgium; Christian Russ; Infineon Technologies AG, Germany

17:10
A4L-A.5 A NEW PRE-DRIVER DESIGN FOR IMPROVING THE ESD PERFORMANCE OF THE HIGH VOLTAGE TOLERANT I/O

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A4L-A.6 ON-CHIP ESD PROTECTION FOR RF I/O: DEVICES, CIRCUITS AND MODELS
Elyse Rosenbaum, Sami Hyvonen, University of Illinois at Urbana-Champaign, USA
A4L-B  Configurable Architecture (Lecture)
Time:  Tuesday, May 24, 2005, 16:10 - 18:10
Place:  Room 401
Co-Chairs: Jshikawa Junji, Renesas
          Myung H. Sunwoo, Ajou University

16:10  A4L-B.1  A METHODOLOGY FOR PARTITIONING DSP APPLICATIONS IN HYBRID
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University of Thessaloniki, Greece; D. Soudris, University of Thrace; C.E. Goutis,
University of Patras, Greece

16:30  A4L-B.2  A NEW APPROACH BASED ON LFF FOR OPTIMIZATION OF DYNAMIC
HARDWARE RECONFIGURATIONS ............................................................ 1210
Zhe Zhou, Sheqin Dong, Xianlong Hong, Tsinghua University, China; Yu-liang Wu, The
Chinese University of Hong Kong; Yoji Kajitani, The University of Kitakyushu, Japan

16:50  A4L-B.3  A 16,000-GATE-COUNT OPTICALLY RECONFIGURABLE GATE ARRAY IN A
STANDARD 0.35µM CMOS TECHNOLOGY .................................................. 1214
Minoru Watanabe, Fuminori Kobayashi, Kyusyu Institute of Technology, Japan

17:10  A4L-B.4  PIPELINING TECHNIQUE FOR ENERGY-AWARE DATAPATHS ............... 1218
Wei-Sheng Huang, Tay-Jyi Lin, Shih-Hao Ou, Chih-Wei Liu, National Chiao Tung
University, Taiwan ROC; Chein-Wei Jen, Industrial Technology Research Institute,
Taiwan ROC

17:30  A4L-B.5  A LOW POWER FPGA ROUTING ARCHITECTURE ................................ 1222
Somshebra Mondal, Seda Ogrenzi Memik, Northwestern University, USA

17:50  A4L-B.6  EFFICIENT HIGH RADIX MODULAR MULTIPLICATION FOR HIGH-SPEED
COMPUTING IN RE-CONFIGURABLE HARDWARE ........................................ 1226
Yi Wang, Jussipekka Leiwo, Thambipillai Srikatan, Nanyang Technological University,
Singapore
SPECIAL SESSION - Video Adaptation & Abstraction (Lecture)

Time: Tuesday, May 24, 2005, 16:10 - 18:10
Place: Room 402
Co-Chairs: Chia-Wen Lin, National Chung-Cheng University
Yap-Peng Tan, Nanyang Technological University

16:10
A4L-C.1 MOTION INFORMATION AND CODING MODE REUSE FOR MPEG-2 TO H.264 TRANSCODING
Zhi Zhou, University of Washington, USA; Shijun Sun, Shawmin Lei, Sharp Laboratories of America; Ming-Ting Sun, University of Washington, USA

16:30
A4L-C.2 EFFICIENT MPEG-2 TO H.264/AVC INTRA TRANSCODING IN TRANSFORM-DOMAIN
Yeping Su, University of Washington, USA; Jun Xin, Anthony Vetro, Huifang Sun, Mitsubishi Electric Research Laboratories, USA

16:50
A4L-C.3 EFFICIENT RATE CONTROL FOR MPEG-2 TO H.264/AVC TRANSCODING
You-Neng Xiao, Hong Lu, Xiangyang Xue, Fudan University, China; Viet-Anh Nguyen, Yap-Peng Tan, Nanyang Technological University, Singapore

17:10
A4L-C.4 R-D OPTIMIZED QUANTIZATION OF H.264 SP-FRAMES FOR BISTREAM SWITCHING UNDER STORAGE CONSTRAINTS
Cheng-Po Chang, Chia-Wen Lin, National Chung Cheng University, Taiwan ROC

17:30
A4L-C.5 FAST MODE DECISION AND MOTION ESTIMATION FOR H.264 WITH A FOCUS ON MPEG-2/H.264 TRANSCODING
Xiaoan Lu, Polytechnic University, USA; Alexis Michael Tourapis, Peng Yin, Jill Boyce, Thomson Inc., USA

17:50
A4L-C.6 OPTIMIZING USER EXPECTATIONS FOR VIDEO SEMANTIC FILTERING AND ABSTRACTION
Ching-Yung Lin, IBM T. J. Watson Research Center, USA; Belle L. Tseng, NEC Labs America
### A4L-D Advanced Circuits (Lecture)

**Time:** Tuesday, May 24, 2005, 16:10 - 18:10  
**Place:** Room 403  
**Co-Chairs:** Malgorzata Chrzanowska-Jeske, *Portland State University*  
Eby Friedman, *University of Rochester*

#### 16:10 A4L-D.1
**Title:** Analytical Crosstalk Noise and Its Induced-Delay Estimation for Distributed RLC Interconnects Under Ramp Excitation
**Authors:** L. M. Coulibaly, H. J. Kadim, *Liverpool JM University, UK*

#### 16:30 A4L-D.2
**Title:** An All-Digital Pulsewidth Control Loop
**Authors:** Yi-Ming Wang, Chang-Fen Hu, Yi-Jen Chen, Jinn-Shyan Wang, *Chung-Cheng University, Taiwan ROC*

#### 16:50 A4L-D.3
**Title:** Design of a New Sense Amplifier Flip-Flop with Improved Power-Delay-Product
**Authors:** Hui Zhang, Pinaki Mazumder, *University of Michigan, USA*

#### 17:10 A4L-D.4
**Title:** A 1.2 V Sense Amplifier for High-Performance Embeddable NOR Flash Memories
**Authors:** A. Cabrini, D. Baderna, A. Rossini, G. Torelli, *University of Pavia, Italy*; G. De Sandre, F. De Santis, M. Pasotti, *STMicroelectronics, Italy*

#### 17:30 A4L-D.5
**Title:** Set and Reset Pulse Characterization in BJT-Selected Phase-Change Memories
**Authors:** F. Bedeschi, *STMicroelectronics, Italy*; E. Bonizzoni, *University of Pavia, Italy*; G. Casagrande, R. Gastaldi, C. Resta, *STMicroelectronics, Italy*; G. Torelli, *University of Pavia, Italy*; D. Zella, *STMicroelectronics, Italy*

#### 17:50 A4L-D.6
**Title:** Decision Feedback Equalization for High-Speed Backplane Data Communications
**Authors:** Jing Chen, Miao Li, Tad Kwasniewski, *Carleton University, Canada*
A4L-E  Analog Modeling, Synthesis & Optimization (Lecture)
Time: Tuesday, May 24, 2005, 16:10 - 18:10
Place: Room 404
Co-Chairs: Janet Melling, Univ of Arizona
Makoto Nagata, Kobe University

16:10 A4L-E.1 INTERCONNECT MODEL REDUCTIONS BY USING THE AORA ALGORITHM WITH
CONSIDERING THE ADJOINT NETWORK ........................................................................1278
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Taiwan ROC; Wu-Shiung Feng, Ming-Hong Lai, Chang Gung University, Taiwan ROC

16:30 A4L-E.2 PARAMETER DOMAIN PRUNING FOR IMPROVING CONVERGENCE OF
SYNTHESIS ALGORITHMS ..........................................................................................1282
Hua Tang, Alex Doboli, State University of New York at Stony Brook, USA

16:50 A4L-E.3 ENRICHING AN ANALOG PLATFORM FOR ANALOG-TO-DIGITAL CONVERTER
DESIGN .........................................................................................................................1286
F. De Bernardinis, P. Nuzzo, P. Terreni, University of Pisa, Italy; A. Sangiovanni
Vincentelli, UC Berkeley

17:10 A4L-E.4 PARAMETRIC MODEL ORDER REDUCTION TECHNIQUE FOR DESIGN
OPTIMIZATION ................................................................................................................1290
Alfred Tze-Mun Leung, Roni Khazaka, McGill University, Canada

17:30 A4L-E.5 DESIGN AUTOMATION OF SINGLE-ENDED LNAs USING SYMBOLIC ANALYSIS ..........1294
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17:50 A4L-E.6 ANALYSIS OF SIMULATION-DRIVEN NUMERICAL PERFORMANCE MODELING
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Time: Tuesday, May 24, 2005, 16:10 - 18:10
Place: Room 405
Co-Chairs: Dariusz Czarkowski, Brooklyn Polytechnic
          Hiroo Sekiya, Chiba University

16:10
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        CONVERTERS FOR ENVELOPE TRACKING IN RF POWER AMPLIFIERS .......... 1302
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        University of Catalunya, Spain; D. Maksimovic, University of Colorado at Boulder, USA

16:30
A4L-F.2 HYBRID TRIGONOMETRIC DIFFERENTIAL EVOLUTION FOR OPTIMIZING
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        Shiyan Hu, Han Huang, Dariusz Czarkowski, Polytechnic University, USA

16:50
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        Y. Berkovich, B. Axelrod, A. Ioinovici, Holon Academic Institute of Technology, Israel

17:10
A4L-F.4 HIGH EFFICIENCY WIDE BANDWIDTH POWER SUPPLIES FOR GSM AND EDGE
        RF POWER AMPLIFIERS ............................................................................ 1314
        Yushan Li, National Semiconductor, USA; Dragan Maksimovic, University of Colorado at
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A4L-F.5 BOOST-BUCK INVERTER VARIABLE STRUCTURE CONTROL FOR GRID-
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        Carlos Meza, Domingo Biel, Juan Martinez, Francesc Guinjoan, Universidad Politecnica
        de Catalunya, Spain

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        Hirotaka Koizumi, Kosuke Kurokawa, Tokyo University of Agriculture and Technology,
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A4L-G  Biomedical Processing (Lecture)
Time:  Tuesday, May 24, 2005, 16:10 - 18:10
Place:  Room 406
Co-Chairs: Katsuya Kondo, University of Hyogo
         Yong Lian, National University of Singapore

16:10
A4L-G.1  MODELING EXTERNAL FEEDBACK PATH OF AN ITE DIGITAL HEARING
INSTRUMENT FOR ACOUSTIC FEEDBACK CANCELLATION..............................1326
Jingbo Yang, Meng Tong Tan, Joseph S. Chang, Nanyang Technolgocial University,
Singapore

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Joachim Neves Rodrigues, Thomas Olsson, Leif Sörmmo, Viktor Öwall, Lund University,
Sweden

16:50
A4L-G.3  AN EFFICIENT ECG DATA COMPRESSION TECHNIQUE BASED ON PREDEFINED
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Hakan Gürkan, Ümit Güz, B. Siddik Yarman, ISIK University, Turkey

17:10
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Zhipeing Lin, Qiuye Zou, Nanyang Technolgocial University, Singapore; Raimund J. Ober,
University of Texas at Dallas, USA

17:30
A4L-G.5  A SCALABLE ARCHITECTURE FOR STREAMING NEURAL INFORMATION FROM
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Kyle E. Thomson, Yasir Suhail, Karim G. Oweiss, Michigan State University, USA

17:50
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Yehya H. Ghallab, Wael Badawy, University of Calgary, Canada
16:10
A4L-H.1 PROBABILISTIC CONGESTION PREDICTION IN HIERARCHICAL QUAD-GRID MODEL
Jin-Tai Yan, Yen-Hsiang Chen, Chia-Wei Wu, Chung Hua University, Taiwan ROC

16:30
A4L-H.2 SMALL CONGESTION EMBEDDING OF SEPARABLE GRAPHS INTO GRIDS OF THE SAME SIZE
Akira Matsubayashi, Kanazawa University, Japan

16:50
A4L-H.3 ON VLSI DECOMPOSITIONS FOR D-ARY DE BRUIJN GRAPHS (EXTENDED ABSTRACT)
Toshinori Yamada, Saitama University, Japan; Hiroyuki Kawakita, Tadashi Nishiyama, Shuichi Ueno, Tokyo Institute of Technology, Japan

17:10
A4L-H.4 APPROXIMATION ALGORITHMS FOR THE RECTILINEAR STEINER TREE PROBLEM WITH OBSTACLES
Makoto Fujimoto, Daisuke Takaifuji, Toshimasa Watanabe, Hiroshima University, Japan

17:30
A4L-H.5 WIRING AREA OPTIMIZATION IN FLOORPLAN-AWARE HIERARCHICAL POWER GRIDS
Jin-Tai Yan, Chia-Wei Wu, Yen-Hsiang Chen, Chung Hua University, Taiwan ROC

17:50
A4L-H.6 TIMING-DRIVEN STEINER TREE CONSTRUCTION BASED ON FEASIBLE ASSIGNMENT OF HIDDEN STEINER POINTS
Jin-Tai Yan, Tzu-Ya Wang, Yu-Cheng Lee, Chung Hua University, Taiwan ROC
16:10  A4L-J.1  A ROBUST BACKGROUND CALIBRATION TECHNIQUE FOR SWITCHED-CAPACITOR PIPELINED ADCS ................................. 1374
Jen-Lin Fan, Jieh-Tsong Wu, National Chiao Tung University, Taiwan ROC

16:30  A4L-J.2  A DIGITAL SELF-CALIBRATION ALGORITHM FOR ADCS BASED ON HISTOGRAM TEST USING LOW-LINEARITY INPUT SIGNALS .................................................. 1378
Le Jin, Degang Chen, Randall Geiger, Iowa State University, USA

16:50  A4L-J.3  A LINEAR-APPROXIMATION TECHNIQUE FOR DIGITALLY-CALIBRATED PIPELINED A/D CONVERTERS .......................................................... 1382
Ding-Lan Shen, Tai-Cheng Lee, National Taiwan University, Taiwan ROC

17:10  A4L-J.4  DESIGN OF A 2-GS/S 8-B SELF-CALIBRATING ADC IN 0.18 µM CMOS TECHNOLOGY .......................................................... 1386
Cristiano Azzolini, Andrea Boni, Alessio Facen, Matteo Parenti, Davide Vecchi, University of Parma, Italy

17:30  A4L-J.5  BACKGROUND CALIBRATION OF INTERLEAVED ANALOG TO DIGITAL CONVERTERS FOR HIGH-SPEED COMMUNICATIONS USING INTERLEAVED TIMING RECOVERY TECHNIQUES .................................................. 1390
Oscar E. Agazzi, Venugopal Gopinathan, Broadcom Corporation, USA

17:50  A4L-J.6  SPECTRAL SHAPING OF TIMING MISMATCHES IN TIME-INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS ............................................. 1394
Christian Vogel, Graz University of Technology, Austria; Dieter Draxelmayr, Infineon Technologies AG, Austria; Gernot Kubin, Graz University of Technology, Austria
A4L-K  Discrete-Time Filter Techniques (Lecture)
Time:  Tuesday, May 24, 2005, 16:10 - 18:10
Place:  Room 502
Co-Chairs:  Joseph Chang, Nanyang Technical University, Singapore
            Jaime Ramirez-Angulo, New Mexico State University

16:10  
A4L-K.1  PROGRAMMABLE SWITCHED-CURRENT FLOATING-GATE CELLS
        Phil Corbishley, Esther Rodriguez-Villegas, Imperial College, London, UK

16:30  
A4L-K.2  TIME-INTERLEAVED SWITCHED-CAPACITOR FILTER FOR RECONFIGURABLE
        TRIPLE-BAND DELTA-SIGMA CONVERTER
        Daeik D. Kim, Martin A. Brooke, Duke University, USA

16:50  
A4L-K.3  A NOVEL CURRENT-CONVEYOR-BASED SWITCHED-CAPACITOR INTEGRATOR
        H. Kaabi, M. R. Jahed Motlagh, A. Ayatollahi, Iran University of Science and
        Technology, Iran

17:10  
A4L-K.4  A NEW MULTIPLY-BY-TWO GAIN-STAGE WITH ENHANCED IMMUNITY TO
        CAPACITOR-MISMATCH
        Hashem Zare-Hoseini, University of Westminster, UK; Omid Shoaei, University of
        Tehran, Iran; Izzet Kale, University of Westminster, UK

17:30  
A4L-K.5  INVERTER-BASED SWITCHED CURRENT CIRCUIT FOR VERY LOW-VOLTAGE
        AND LOW-POWER APPLICATIONS
        Marcio C. Schneider, Universidade Federal de Santa Catarina, Brazil; Fathi A. Farag,
        Zagazig University; Carlos Galup-Montoro, Universidade Federal de Santa Catarina,
        Brazil

17:50  
A4L-K.6  A HIGH SPEED, HIGH RESOLUTION, LOW VOLTAGE CURRENT MODE SAMPLE
        AND HOLD
        Omid Rajaee, Mehrdad Sharif Bakhtiar, Sharif University of Technology, Iran
16:10  A4L-L.1  AN IMPROVED ALGORITHM FOR MAXIMUM-LIKELIHOOD BASED APPROACH FOR A MULTITARGET TRACKING PROBLEM ............................................................ 1421
Liang Chen, University of Northern British Columbia, Canada; Qiang Hua, Hebei University, China; H. K. Kwan, University of Windsor, Canada

16:30  A4L-L.2  OPTIMAL PERIODIC SAMPLING SEQUENCES FOR NEARLY-ALIAS-FREE DIGITAL SIGNAL PROCESSING .................................................................................. 1425
Andrzej Tarczynski, Dongdong Qu, University of Westminster, UK

16:50  A4L-L.3  NORMALIZED CONFIDENCE FACTORS FOR ROBUST DIRECTION OF ARRIVAL ESTIMATION .................................................................................. 1429
Tuomo W. Pitinen, Tampere University of Technology, Finland

17:10  A4L-L.4  AN EFFICIENT METHOD FOR ESTIMATION OF AUTOREGRESSIVE SIGNALS IN NOISE ............................................................................................. 1433
Wei Xing Zheng, University of Western Sydney, Australia

17:30  A4L-L.5  SYMBOL-RATE ESTIMATION BASED ON FILTER BANK .................................................................................. 1437
Zaihe Yu, Yun Q. Shi, New Jersey Institute of Technology, USA; Wei Su, US Army RDECOM CERDEC

17:50  A4L-L.6  PILOT-AIDED DOA ESTIMATION FOR CDMA COMMUNICATION SYSTEMS .................................................................................. 1441
N. Y. Wang, P. Agathoklis, A. Antoniou, University of Victoria, Canada
Digital Signal Processing Algorithm Implementation I (Lecture)

Time: Tuesday, May 24, 2005, 16:10 - 18:10
Place: Room 504
Co-Chairs: Nobuhiko Sugino, Tokyo Institute of Technology
Tsung-Han Tsai, National Central University

16:10
A4L-M.1 NEW COST-EFFECTIVE VLSI IMPLEMENTATION OF MULTIPLIERLESS FIR FILTER USING COMMON SUBEXPRESSION ELIMINATION
Yasuhiro Takahashi, Michio Ykoyama, Yamagata University, Japan

16:30
A4L-M.2 IMPLEMENTATION OF LOW-COMPLEXITY FIR FILTERS USING SERIAL ARITHMETIC
Kenny Johansson, Oscar Gustafsson, Lars Wenhammar, Linköping University, Sweden

16:50
A4L-M.3 A LOW POWER DECIMATION FILTER ARCHITECTURE FOR HIGH-SPEED SINGLE-BIT SIGMA-DELTA MODULATION
Oscar Gustafsson, Henrik Ohlsson, Linköping University, Sweden

17:10
A4L-M.4 A HIGH PERFORMANCE DISTRIBUTED-PARALLEL-PROCESSOR ARCHITECTURE FOR 3D IIR DIGITAL FILTERS
Arjuna Madanayake, Len Bruton, University of Calgary, Canada

17:30
A4L-M.5 A VLSI ARCHITECTURE FOR A HIGH-SPEED COMPUTATION OF THE 1-D DISCRETE WAVELET TRANSFORM
Chengjun Zhang, Chunyan Wang, M. Omair Ahmad, Concordia University, Canada

17:50
A4L-M.6 MEMORY ACCESS OVERHEAD REDUCTION FOR A DIGITAL COLOR COPIER IMPLEMENTATION USING A VLIW DIGITAL SIGNAL PROCESSOR
Moonseok Kang, Wonyong Sung, Seoul National University, Korea
A4L-N  Chaos & Bifurcation in Circuits & Systems (Lecture)
Time:      Tuesday, May 24, 2005, 16:10 - 18:10
Place:     Room 505
Co-Chairs: Tohru Kohda, Kyushu University
            Michael Tse, HK Polytechnic University

16:10
A4L-N.1  HORSESHOES, HOMOCLINIC CONNECTIONS AND GLOBAL CHAOS IN
          CURRENT-MODE CONTROLLED DC/DC CONVERTERS ........................................... 1469
          Dong Dai, Hong Kong Polytechnic University, Hong Kong; Yue Ma, Tokushima
          University, Japan; Chi K. Tse, Hong Kong Polytechnic University, Hong Kong

16:30
A4L-N.2  N-SCROLL CHAOTIC ATTRACTORS FROM A GENERAL JERK CIRCUIT ....................... 1473
          Simin Yu, Guangdong University of Technology, China; Jinhu Lu, Chinese Academy of
          Sciences, China; Henry Leung, University of Calgary, Canada; Guanrong Chen, City
          University of Hong Kong

16:50
A4L-N.3  SOLVABLE 2-DIMENSIONAL RATIONAL CHAOTIC MAP DEFINED BY JACOBIAN
          ELLIPTIC FUNCTIONS ........................................................................... 1477
          Tohru Kohda, Aya Kato, Kyushu University, Japan

17:10
A4L-N.4  BACK PROPAGATION LEARNING OF NEURAL NETWORKS WITH CHAOTICALLY-
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          Yoko Uwate, Yoshifumi Nishio, Tokushima University, Japan

17:30
A4L-N.5  ON TWO-PARAMETER NON-SMOOTH BIFURCATIONS IN POWER CONVERTERS .... 1485
          F. Angulo, Universidad Nacional de Colombia, sede de Manizales; M. di Bernardo, S. J.
          Hogan, P. Kowalczyk, University of Bristol, UK; G. Olivar, Technical University of
          Catalonia, Spain

17:50
A4L-N.6  EXPERIMENTAL PERFORMANCE EVALUATION OF A LOW-EMI CHAOS-BASED
          CURRENT-PROGRAMMED DC/DC BOOST CONVERTER .................................... 1489
          Michele Balestra, Marco Lazzarini, Gianluca Setti, University of Ferrara, Italy; Riccardo
          Rovatti, University of Bologna, Italy
**A4L-P** Efficient Implementation of AVC/H.264 (Lecture)

*Time: Tuesday, May 24, 2005, 16:10 - 18:10*

*Place: Nogiggiku Room, Portopia Hotel*

*Co-Chairs: Oscar Au, Hong Kong University of Science and Technology*

Nam Ling, Santa Clara University

16:10

**A4L-P.1** AN ADAPTIVE FAST FULL SEARCH MOTION ESTIMATION ALGORITHM FOR H.264

Chen-Fu Lin, Jin-Jang Leou, National Chung Cheng University, Taiwan ROC

16:30

**A4L-P.2** TRANSFORM-DOMAIN INTRA PREDICTION FOR H.264

Chen Chen, Ping-Hao Wu, Homer Chen, National Taiwan University, Taiwan ROC

16:50

**A4L-P.3** AN IMPROVED FRAME AND MACROBLOCK LAYER BIT ALLOCATION SCHEME FOR H.264 RATE CONTROL

Minqiang Jiang, Nam Ling, Santa Clara University, USA

17:10

**A4L-P.4** FAST MULTI-FRAME MOTION ESTIMATION FOR H.264 AND ITS APPLICATIONS TO COMPLEXITY-AWARE STREAMING

Shu-Fa Lin, Meng-Ting Lu, Homer Chen, National Taiwan University, Taiwan ROC;
Chia-Ho Pan, Industrial Technology Research Institute, Taiwan ROC

17:30

**A4L-P.5** FAST THREE STEP INTRA PREDICTION ALGORITHM FOR 4X4 BLOCKS IN H.264

Chao-Chung Cheng, Tian-Sheuan Chang, National Chiao Tung University, Taiwan ROC

17:50

**A4L-P.6** FAST BLOCK MOTION ESTIMATION WITH EARLY ACCEPTANCE TECHNIQUE IN H.264/JVT

Chi-Wai Lam, Lai-Man Po, City University of Hong Kong
A4L-Q  Optical Circuits & Systems (Lecture)
Time:   Tuesday, May 24, 2005, 16:10 - 18:10
Place:  Sumire Room, Portopia Hotel
Co-Chairs: Anthony Chan Caruson, University of Toronto
Naoya Wada, NICT

16:10
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Takayuki Yamashita, NHK; Kazuhiisa Haeiwa, Hiroshima City University, Japan;
Toshihiro Negishi, Izuru Murasaki, NHK; Yoshikazu Toba, Masatoshi Onizawa, NEC
Tokin, Japan

16:30
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Jonathan Sewter, Anthony Chan Caruson, University of Toronto, Canada

16:50
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Hai Qi Liu, Wang Ling Goh, Liter Siek, Nanyang Technolgocial University, Singapore

17:10
A4L-Q.4 FOUR-CHANNEL CMOS PHOTORECEIVER ARRAY FOR PARALLEL OPTICAL INTERCONNECTS ...................................................................................... 1529
Ju-Hyoung Mun, Sung Min Park, Ewha Womans University, Korea; Myung-Ryong
Nam, Satellite Technology Research Center, KAIST, Korea

17:30
A4L-Q.5 A SWITCHED DELAY LINE BASED OPTICAL SWITCH ARCHITECTURE WITH A BYPASS LINE ................................................................................. 1533
Ho-Ting Wu, Kai-Wei Ke, National Taiwan University of Technology, Taiwan ROC; Wang-Rong Chang, Hui-Tang Lin, National Cheng Kung University, Taiwan ROC

17:50
A4L-Q.6 A 400MBPS CMOS SPATIALLY-MODULATED PHOTORECEIVER FOR OPTICAL STORAGE ................................................................. 1537
Euhun Chong, Khoman Phang, University of Toronto, Canada
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Time:  Tuesday, May 24, 2005, 16:10 - 18:10
Place:  Tsutsuji Room, Portopia Hotel
Co-Chairs: Pau-Choo Chung, National Cheng Kung University
          Jeng-Shyang Pan, National Kaohsiung University of Applied Sciences

16:10
A4L-R.1  MIRROR: AN INTERACTIVE CONTENT BASED IMAGE RETRIEVAL SYSTEM ................. 1541
         Ka-Man Wong, City University of Hong Kong; Kwok-Wai Cheung, Chu Hai College,
         Hong Kong; Lai-Man Po, City University of Hong Kong

16:30
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         Yingqing Zhao, C.-C. Jay Kuo, University of Southern California, USA

16:50
A4L-R.3  PROGRAM SEGMENTATION FOR TV VIDEOS .......................................................... 1549
         Liuhong Liang, Hong Lu, Xiangyang Xue, Fudan University, China; Yap-Peng Tan,
         Nanyang Technological University, Singapore

17:30
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         Huang-Chia Shih, Chung-Lin Huang, National Tsing Hua University, Taiwan ROC

17:50
A4L-R.6  A NOVEL BP-BASED IMAGE RETRIEVAL SYSTEM .................................................... 1557
         Jun-Hua Han, De-Shuang Huang, Chinese Academy of Sciences, China
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<td>Salvatore Pennisi, University of Catania, Italy</td>
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<td>Khanittha Kaewdang, Wanlop Surakampontorn, King Mongkut's Institute of Technology, Ladkrabang, Thailand; Nobuo Fujii, Tokyo Institute of Technology, Japan</td>
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<td>A NOVEL LOW-VOLTAGE CROSS-COUPLED PASSIVE SAMPLING BRANCH FOR RESET- AND SWITCHED-OPAMP CIRCUITS</td>
<td>Sai-Weng Sin, University of Macau; Seng-Pan U, Chipidea Microelectronics, Macao; R.P. Martins, University of Macau</td>
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<td>CURRENT-MODE UNIVERSAL Biquad CIRCUIT USING MO-OTAS AND DO-CCII</td>
<td>Takao Tsukutani, Matsue National College of Technology, Japan; Yasuaki Sumi, Tottori University, Japan; Masami Higashimura, Matsue National College of Technology, Japan; Yutaka Fukui, Tottori University, Japan</td>
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A4P-T1 Wideband Amplifiers (Poster)
Time: Tuesday, May 24, 2005, 16:10 - 18:10
Place: Reception Hall - Area 2
Chair: Wouter Serdijn, Delft University of Technology, the Netherlands

A4P-T1 A LOW-POWER METHOD ADDING CONTINUOUS VARIABLE GAIN TO AMPLIFIERS
Thomas Halvorsrød, Norwegian University of Science and Technology, Norway; Øyvind Birkenes, Christian Eichrodt, Chipcon AS, Norway

A4P-T2 DESIGN CONSIDERATION FOR LOWERING SENSITIVITY TO OUT OF BAND INTERFERENCE OF NEGATIVE FEEDBACK AMPLIFIERS
Emil Totev, Chris Verhoeven, Delft University of Technology, The Netherlands

A4P-T3 A 2.4 GHZ 82 DBΩ FULLY DIFFERENTIAL CMOS TRANSIMPEDEANCE AMPLIFIER FOR OPTICAL RECEIVER BASED ON WIDE-SWING CASCODE TOPOLOGY
Yanjie Wang, Rabin Raut, Concordia University, Canada

A4P-T4 CASCADED DOUBLE-STAGE CONFIGURATION FOR HIGH-PERFORMANCE BROADBAND AMPLIFICATION IN CMOS
Apisak Worapisheet, Ittipat Roopkom, Mahanakorn University of Technology, Thailand

A4P-T5 INFLUENCE OF FREQUENCY COMPENSATION ON THE LINEARITY OF NEGATIVE FEEDBACK AMPLIFIERS
Koen van Hartingsveldt, Chris Verhoeven, Delft University of Technology, The Netherlands; John Willms, National Semiconductor BV, The Netherlands

A4P-T6 A 3 GB/S 80 DB CMOS DIFFERENTIAL TRANSIMPEDEANCE AMPLIFIER FOR OPTICAL COMMUNICATION SYSTEMS
Wacharapol Pongpait, Varakorn Kasemmuwan, King Mongkut’s Institute of Technology, Ladkrabang, Thailand; Hyung Keun Ahn, Konkuk University, Korea

A4P-T7 POWER DEPENDENCE OF FEEDBACK AMPLIFIERS ON OPAMP ARCHITECTURE
Vipul Katyal, Yu Lin, Randall L. Geiger, Iowa State University, USA

A4P-T8 DIGITALLY CONTROLLED FULLY DIFFERENTIAL CURRENT CONVEYOR: CMOS REALIZATION AND APPLICATIONS
Soliman Mahmoud, Mohammed A. Hashiash, Ahmed M Soliman, Cairo University, Egypt
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Place:   Reception Hall - Area 3
Chair:   Yuke Wang, University of Texas at Dallas

A4P-U.1  A SUB-WORD-PARALLEL GALOIS FIELD MULTIPLY-ACCUMULATE UNIT FOR
DIGITAL SIGNAL PROCESSORS
Sourav Roy, Analog Devices, India

A4P-U.2  A CONFIGURABLE DUAL MODULI MULTI-OPERAND MODULO ADDER
Chip Hong Chang, Shibu Menon, Bin Cao, Thambipillai Srikanthan, Nanyang
Technological University, Singapore

A4P-U.3  AN MCML FOUR-BIT RIPPLE-CARRY ADDER DESIGN IN 1 GHZ RANGE
Shahnam Khabiri, Maitham Shams, Carleton University, Canada

A4P-U.4  LOW POWER PARALLEL MULTIPLIER WITH COLUMN BYPASSING
Min-Chen Wen, Sying-Jyan Wang, Yen-Nan Lin, National Chung Hsing University,
Taiwan ROC

A4P-U.5  DESIGN OF POWER-AWARE MULTIPLIER WITH GRACEFUL QUALITY-POWER
TRADE-OFFS
Jieh-Hwang Yen, Lan-Rong Dung, National Chiao Tung University, Taiwan ROC; Chi-
Yuan Shen, UMC Corp., Taiwan

A4P-U.6  EQUALIZING DATA-PATH FOR PROCESSING SPEED DETERMINATION IN BLOCK
LEVEL PIPELINING
Xiaoyao Liang, Akshay Athalye, Sangjin Hong, Stony Brook University, USA
A4P-V
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Time:  Tuesday, May 24, 2005, 16:10 - 18:10
Place: Reception Hall - Area 4
Chair:  Mircea R. Stan, University of Virginia

A4P-V.1 DUAL SENSE AMPLIFIED BIT LINES (DSABL) ARCHITECTURE FOR LOW-POWER SRAM DESIGN
Ramy E. Aly, Magdy A. Bayoumi, Mohamed Elgamel, University of Louisiana at Lafayette, USA

A4P-V.2 A LOW-LEAKAGE TWIN-PRECISION MULTIPLIER USING RECONFIGURABLE POWER GATING
Magnus Sjölander, Mindaugas Drazdziulis, Per Larsson-Edefors, Henrik Eriksson, Chalmers University of Technology

A4P-V.3 AN ENERGY-EFFICIENT SKEW COMPENSATION TECHNIQUE FOR HIGH-SPEED SKEW-SENSITIVE SIGNALING
Lei Wang, University of Connecticut, USA

A4P-V.4 AREA, POWER, AND PIN EFFICIENT BUS TRANSCEIVER USING MULTI-BIT-DIFFERENTIAL SIGNALING
Donald M. Chiarulli, Jason D. Bakos, Joel R. Martin, Steven P. Levitan, University of Pittsburgh, USA

A4P-V.5 ENHANCING THE EFFICIENCY OF CLUSTER VOLTAGE SCALING TECHNIQUE FOR LOW-POWER APPLICATION
Behnam Amelifar, Ali Afzali-Kusha, University of Tehran, Iran; Ahmad Khademzadeh, Iran University of Science and Technology, Iran

A4P-V.6 A LOW-POWER HIGH-SFDR CMOS DIRECT DIGITAL FREQUENCY SYNTHESIZER
Jinn-Shyan Wang, Shiang-Jiun Lin, Chingwei Yeh, Chung-Cheng University, Taiwan ROC

A4P-V.7 DOMINO LOGIC WITH AN EFFICIENT VARIABLE THRESHOLD VOLTAGE KEEPER
A. Amirabadi, Y. Mortazavi, N. Moezzi Madani, A. Afzali-Kusha, University of Tehran, Iran; M. Nourani, University of Texas at Dallas, USA

A4P-V.8 A LOW DYNAMIC POWER AND LOW LEAKAGE POWER CMOS SQUARE ROOT CIRCUIT
Tadayoshi Enomoto, Nobuaki Kobayashi, Chuo University, Japan

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Digital Signal Processing Applications III (Poster)

Time: Tuesday, May 24, 2005, 16:10 - 18:10
Place: Reception Hall - Area 5
Chair: Yuan-Fei Lin, National Chiao Tung University

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Jianfeng Chen, Koksoon Phua, Louis Shue, Hanwu Sun, Institute for Infocomm Research, Singapore

A4P-W.2 A COMBINED TDA/FDA ADAPTIVE SCHEMA FOR STEREOPHONIC ACOUSTIC ECHO CANCELLATION
M. Khasawneh, K. C. Mayyas, Jordan University of Science & Technology, Jordan; R. M. Shalabi, Nokia, Inc., UAE; M. I. Haddad, ETISALAT Telecom, UAE

A4P-W.3 IMAGE ENCRYPTION USING PROGRESSIVE CELLULAR AUTOMATA SUBSTITUTION AND SCAN
Rong-Jian Chen, Wen-Kai Lu, Jui-Lin Lai, National United University, Taiwan ROC

A4P-W.4 STUDY OF A LEAST-SQUARES TYPE METHOD FOR NOISY FIR FILTERING
Wei Xing Zheng, University of Western Sydney, Australia

A4P-W.5 OPTIMAL USER WEIGHTING FUSION IN DWT DOMAIN ON-LINE SIGNATURE VERIFICATION
Isao Nakanishi, Hiroyuki Sakamoto, Yoshio Itoh, Yutaka Fukui, Tottori University, Japan

A4P-W.6 A HARDWARE GENERATOR FOR MULTI-POINT DISTRIBUTED RANDOM VARIABLES
Filippo Martini, Massimo Piccardi, Nicola Bruti Liberati, Eckhard Platen, University of Technology, Sydney, Australia

A4P-W.7 DIRECT-DIGITAL SYNTHESIS USING DELTA-SIGMA MODULATED SIGNALS
Yuichiro Orino, Minoru Kuribayashi Kurosawa, Tokyo Institute of Technology, Japan; Takashi Katagiri, Sutekina Inc., Japan
A4P-X  Digital Signal Processing for Communications III (Poster)
Time:  Tuesday, May 24, 2005, 16:10 - 18:10
Place:  Reception Hall - Area 6
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A4P-X.2 DIVERSITY GAIN'S INFLUENCE ON MIMO'S DETECTION . . . 1714
Hui Zhao, Kan Zheng, Wenbo Wang, Beijing Univ. of Posts & Telecommunications, China

A4P-X.3 MULTIUSER SCHEDULING FOR DOWNLINK IN MULTI-ANTENNA WIRELESS
SYSTEMS .................................................................................. 1718
Deepali Arora, Panajotis Agathoklis, University of Victoria, Canada

A4P-X.4 ROBUST ADAPTIVE CHANNEL ESTIMATION OF OFDM SYSTEMS IN TIME-
VARYING NARROWBAND INTERFERENCE ........................................... 1722
Zhiguo Zhang, Shing-Chow Chan, Hui Cheng, The University of Hong Kong

A4P-X.5 JOINT FREQUENCY OFFSET ESTIMATION AND MULTIUSER DETECTION USING
GENETIC ALGORITHM IN MC-CDMA .................................................. 1726
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Yu-Hao Chang, Xiaoli Yu, University of Southern California, USA

A4P-X.7 PERFORMANCE OF THE PULSE PAIR METHOD WITH AN OPTIMAL LAG VALUE
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Saman S. Abeysekera, Zhi Wang, Nanyang Technological University, Singapore

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A4P-Y  Sensory Systems, Chemical & Olfactory Sensors (Poster)
Time:  Tuesday, May 24, 2005, 16:10 - 18:10
Place:  Reception Hall - Area 7
Chair:  Denise Wilson, University of Washington

A4P-Y.1 INTEGRATED MIXED-SIGNAL OPTOELECTRONIC SYSTEM-ON-A-CHIP SENSOR
Daeil D. Kim, Duke University, USA; Mikkel A. Thomas, Jeffrey J. Lillie, Karla S. Dennis,
Benita M. Comeau, Georgia Institute of Technology, USA; Martin A. Brooke, Nan M.
Jokerst, Duke University, USA; Stephen E. Ralph, Clifford L. Henderson; Georgia
Institute of Technology, USA

A4P-Y.2 A 60NS 500X12 0.35μM CMOS LOW-POWER SCANNING READ-OUT IC FOR
CRYOGENIC INFRA-RED SENSORS
F. Serra-Graells, B. Misischi, Institut de Microelectronica de Barcelona - CNM- CSIC,
Spain; E. Casanueva, C. Méndez, Indra Sistemas S.A., Spain; L. Terés, Institut de
Microelectronica de Barcelona - CNM- CSIC, Spain

A4P-Y.3 INSTRUMENTATION OF YSZ OXYGEN SENSOR CALIBRATION IN LIQUID LEAD-
BISMUTH EUTECTIC
Xiaolong Wu, Jian Ma, Yingtao Jiang, Bingmei Fu, University of Nevada, Las Vegas,
USA; Wei Hang, Jinsuo Zhang, Ning Li, Los Alamos National Laboratory, USA

A4P-Y.4 AN AUTOMATIC ACOUSTIC BATHROOM MONITORING SYSTEM
Jianfeng Chen, Jianmin Zhang, Alvin Harvey Kam, Louis Shue, Institute for Infocomm
Research, Singapore

A4P-Y.5 A PWM DPS WITH PIXEL-LEVEL RECONFIGURABLE 4/8-BIT COUNTER/SRAM
Yung Yat-Fong, Amine Bermak, Hong Kong University of Science and Technology, Hong
Kong

A4P-Y.6 SENSOR ARRAY FOR MULTIPLE EMISSION GAS MEASUREMENTS
Matti Kutila, Jouko Viitanen, VTT, Finland

A4P-Y.7 PULSE-BASED INTERFACE CIRCUITS FOR SPR SENSING SYSTEMS
Lisa E. Hansen, Matthew M. W. Johnston, Denise M. Wilson, University of Washington,
USA
SPECIAL SESSION - Networks-on-Chip (NoCs) Theory & Applications I (Lecture)

Time: Wednesday, May 25, 2005, 09:00 - 11:00

Place: Room 301

Co-Chairs: Giovanni De Micheli, EPFL
André Ivanov, University of British Columbia

09:00

**B1L-A.1** NETWORK-ON-CHIP-CENTRIC APPROACH TO INTERLEAVING IN HIGH THROUGHPUT CHANNEL DECODERS ................................................................. 1766
Christian Neeb, Michael Thul, Norbert Wehn, University of Kaiserslautern, Germany

09:20

**B1L-A.2** POWER ANALYSIS OF LINK LEVEL AND END-TO-END DATA PROTECTION IN NETWORKS ON CHIP ................................................................. 1770
Axel Jantsch, Robert Lauter, Arseni Vitkowski, Royal Institute of Technology, Sweden

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**B1L-A.3** EFFECT OF TRAFFIC LOCALIZATION ON ENERGY DISSIPATION IN NOC-BASED INTERCONNECTS ................................................................. 1774
Partha Pande, Cristian Grecu, Michael Jones, André Ivanov, Res Saleh, University of British Columbia, Canada

10:00

**B1L-A.4** A METHODOLOGY FOR DESIGN, MODELING, AND ANALYSIS OF NETWORKS-ON-CHIP ................................................................. 1778
Jiang Xu, Wayne Wolf, Princeton University, USA; Joerg Henkel, University of Karlsruhe; Srimat Chakradhar, NEC American Labs Inc.

10:20

**B1L-A.5** QUANTITATIVE MODELLING AND COMPARISON OF COMMUNICATION SCHEMES TO GUARANTEE QUALITY-OF-SERVICE IN NETWORKS-ON-CHIP ................................................................. 1782
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10:40

**B1L-A.6** VLSI ARCHITECTURE BASED ON PACKET DATA TRANSFER SCHEME AND ITS APPLICATION ................................................................. 1786
Yuya Homma, Michitaka Kameyama, Tohoku University, Japan; Yoshichika Fujiioka, Nobuhiro Tomabechi, Hachinohe Institute of Technology, Japan
09:00
B1L-B.1 SINGLE REFERENCE FRAME MULTIPLE CURRENT MACROBLOCKS SCHEME FOR MULTI-FRAME MOTION ESTIMATION IN H.264/AVC
Tung-Chien Chen, Yu-Wen Huang, Chuan-Yung Tsai, Chao-Tsung Huang, Liang-Gee Chen, National Taiwan University, Taiwan ROC

09:20
B1L-B.2 A NOVEL VLSI ARCHITECTURE FOR VBSME IN MPEG-4 AVC/H.264
Cao Wei, Mao Zhi Gang, Harbin Institute of Technology, China

09:40
B1L-B.3 ARCHITECTURE OF GLOBAL MOTION COMPENSATION FOR MPEG-4 ADVANCED SIMPLE PROFILE
Yi-Hau Chen, Ching-Yeh Chen, Liang-Gee Chen, National Taiwan University, Taiwan ROC

10:00
B1L-B.4 COMBINED 2-D TRANSFORM AND QUANTIZATION ARCHITECTURES FOR H.264 VIDEO CODERS
Heng-Yao Lin, Yi-Chih Chao, Che-Hong Chen, Bin-Da Liu, Jar-Ferr Yang, National Cheng Kung University, Taiwan ROC

10:20
B1L-B.5 COMBINED FRAME MEMORY ARCHITECTURE FOR MOTION COMPENSATION IN VIDEO DECODING
Nelson Chang, Tian-Sheuan Chang, National Chiao Tung University, Taiwan ROC

10:40
B1L-B.6 AN H.264/AVC DECODER WITH 4X4-BLOCK LEVEL PIPELINE
Ting-An Lin, Sheng-Zen Wang, Tsu-Ming Liu, Chen-Yi Lee, National Chiao Tung University, Taiwan ROC
B1L-C SPECIAL SESSION - Low Complexity Digital Filter Design Techniques & Their Applications (Lecture)

Time: Wednesday, May 25, 2005, 09:00 - 11:00
Place: Room 402
Co-Chairs: Oscar Gustafsson, Linkoping University
Yong Lian, National University of Singapore

09:00
B1L-C.1 MULTIPLICATION BY TWO INTEGERS USING THE MINIMUM NUMBER OF ADDERS
Andrew Dempster, University of Westminster, UK; Malcolm Macleod, QinetiQ Ltd

09:20
B1L-C.2 SIGNED POWER-OF-TWO ALLOCATION SCHEME FOR THE DESIGN OF LATTICE ORTHOGONAL FILTER BANKS
Ya Jun Yu, Yong Ching Lim, Nanyang Technolgocial University, Singapore

09:40
B1L-C.3 I2CRA: CONTENTION RESOLUTION ALGORITHM FOR INTRA- AND INTER-COEFFICIENT COMMON SUBEXPRESSSION ELIMINATION
Fei Xu, Chip-Hong Chang, Ching-Chuen Jong, Nanyang Technolgocial University, Singapore

10:00
B1L-C.4 DESIGN AND IMPLEMENTATION OF MULTIPLIERLESS ADJUSTABLE FRACTIONAL-DELAY ALL-PASS FILTERS
Juha Yli-Kaakinen, Tapio Saramäki, Tampere University of Technology, Finland

10:20
B1L-C.5 DESIGN OF FIR DIGITAL FILTERS WITH DISCRETE COEFFICIENTS VIA CONVEX RELAXATION
Wu-Sheng Lu, University of Victoria, Canada

10:40
B1L-C.6 FURTHER COMPLEXITY REDUCTION OF PARALLEL FIR FILTERS
Chao Cheng, Keshab Parhi, University of Minnesota, USA
B1L-D Clocking and I/O Circuits (Lecture)
Time: Wednesday, May 25, 2005, 09:00 - 11:00
Place: Room 403
Co-Chairs: Shyh-Jye Jou, Nat'l Chiao Tung Univ
Gerald E. Sobelman, Univ. of Minnesota

09:00
B1L-D.1 GLITCH-FREE DISCRETELY PROGRAMMABLE CLOCK GENERATION ON CHIP .......... 1839
Maurice Meijer, Francesco Pessolano, Jose Pineda de Gyvez, Philips Research Labs, The Netherlands

09:20
B1L-D.2 A THREE-LEVEL TOGGLE-AVOID BUS SIGNALING SCHEME ........................................ 1843
Yan Zhang, Travis Blalock, Mircea Stan, University of Virginia, USA

09:40
B1L-D.3 A 1.2V MULTI GB/S/PIN MEMORY INTERFACE CIRCUITS WITH HIGH LINEARITY AND LOW MISMATCH ......................................................... 1847
Tae-Hyoung Kim, Uk-Rae Cho, Hyun-Geun Byun, Samsung Electronics, Korea

10:00
B1L-D.4 A DISTRIBUTED FIFO SCHEME FOR ON CHIP COMMUNICATION ....................... 1851
Jabulani Nyathi, Ray Robert Ill Rydberg, Jose G. Delgado-Frias, Washington State University, USA

10:20
B1L-D.5 A MULTIFUNCTIONAL HIGH-VOLTAGE DRIVER CHIP FOR LOW-POWER MOBILE DISPLAY SYSTEMS ............................................................. 1855
Jan Doutreloigne, Miguel Vermandel, Herbert De Smet, Andre Van Calster, University of Gent, Belgium

10:40
B1L-D.6 DESIGN ON MIXED-VOLTAGE I/O BUFFER WITH BLOCKING NMOS AND DYNAMIC GATE-CONTROLLED CIRCUIT FOR HIGH-VOLTAGE-TOLERANT APPLICATIONS .......................................................... 1859
Ming-Dou Ker, Shih-Lun Chen, Chia-Sheng Tsai, National Chiao Tung University, Taiwan ROC
B1L-E  Placement & Routing I (Lecture)
Time: Wednesday, May 25, 2005, 09:00 - 11:00
Place: Room 404
Co-Chairs: Masahiro Fukui, Ritsumeikan University
Patrick Madden, Binghamton Univ

09:00
B1L-E.1 PERFORMANCE CONSTRAINED FLOORPLANNING BASED ON PARTIAL CLUSTERING
Yuchun Ma, Xianlong Hong, Sheqin Dong, Song Chen, Tsinghua University, China;
Chung-Kuan Cheng, UCSD

09:20
B1L-E.2 WIRE-DRIVEN MICROARCHITECTURAL DESIGN SPACE EXPLORATION
Mongkol Ekpanyapong, Sung Kyu Lim, Chinnakrishnan Ballapuram, Hsien-Hsin S. Lee,
Georgia Institute of Technology, USA

09:40
B1L-E.3 INTEGRATED ROUTING RESOURCE ASSIGNMENT FOR RLC CROSSTALK MINIMIZATION
Yici Cai, Bin Liu, Qiang Zhou, Xianlong Hong, Tsinghua University, China

10:00
B1L-E.4 PLACEMENT FOR THE RECONFIGURABLE DATAPATH ARCHITECTURE
Hsin-Ya Lai, Yen-Tai Lai, Chia-Nah Yen, National Cheng Kung University, Taiwan ROC

10:20
B1L-E.5 SIMPLE YET EFFECTIVE ALGORITHMS FOR BLOCK AND I/O BUFFER PLACEMENT IN FLIP-CHIP DESIGN
Hao-Yueh Hsieh, Ting-Chi Wang, National Tsing Hua University, Taiwan ROC

10:40
B1L-E.6 FIXED-OUTLINE FLOORPLANNING WITH CONSTRAINTS THROUGH INSTANCE AUGMENTATION
Rong Liu, Sheqin Dong, Xianlong Hong, Tsinghua University, China; Yoji Kajitani, The University of Kitakyushu, Japan
Charge Pumps (Lecture)

Time: Wednesday, May 25, 2005, 09:00 - 11:00
Place: Room 405
Co-Chairs: Wing Hung Ki, Hong Kong University of Science and Technology
          Shinsaku Mori, Nippon Institute of Technology

09:00  B1L-F.1  HIGH LIGHT-LOAD EFFICIENCY CHARGE PUMPS ........................................1887
Christian Falconi, Giancarlo Savone, Arnaldo D'Amico, University of Tor Vergata, Italy

09:20  B1L-F.2  EFFICIENCY COMPARISON BETWEEN DOUBLER AND DICKSON CHARGE
            PUMPS ...........................................................................1891
Alessandro Cabrini, Davide Baderna, Guido Torelli, University of Pavia, Italy; Marco
          Pasotti, STMicroelectronics, Italy

09:40  B1L-F.3  CHARGE REDISTRIBUTION LOSS CONSIDERATION IN OPTIMAL CHARGE PUMP
            DESIGN ...........................................................................1895
Feng Su, Wing-Hung Ki, Chi-Ying Tsui, Hong Kong University of Science and
          Technology, Hong Kong

10:00  B1L-F.4  A 5V CHARGE PUMP IN A STANDARD 1.8V 0.18µM CMOS PROCESS ..............1899
Tawfique Hasan, University of New South Wales, Australia; Torsten Lehmann, The
          University of New South Wales, Australia; Chee Yee Kwok, University of New South
          Wales, Australia

10:20  B1L-F.5  HEAP CHARGE PUMP OPTIMISATION BY A TAPERED ARCHITECTURE ..........1903
Riccardo Arona, Edoardo Bonizzoni, Franco Maloberti, Guido Torelli, University of Pavia,
          Italy

10:40  B1L-F.6  GATE CONTROL STRATEGIES FOR HIGH EFFICIENCY CHARGE PUMPS ........1907
Feng Su, Wing-Hung Ki, Chi-Ying Tsui, Hong Kong University of Science and
          Technology, Hong Kong