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B6P-V.2  A 2.5 Gb/s CMOS Burst-Mode Limiting Amplifier for GPON System
Chueh-Hao Yu, Industrial Technology Research Institute; Day-Uei Li, Industrial Technology Research Institute

B6P-V.3  50GHz Double-Balanced Up-Conversion Mixer using CMOS 90nm Process
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B6P-V.4  A 3.8-Gb/s CMOS Laser Driver with Automatic Power Control using Thermistors
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B6P-V.5  A New CMOS BPSK Modulator with Optimal Transaction Bandwidth Control
A. Tang, Ryerson University; F. Yuan, Ryerson University; E. Law, Ryerson University

B6P-W  Communications Circuit Design II (Poster)
Time:  Tuesday, May 29, 2007, 14:30 - 16:20
Place:  Poster Area 9
Chair(s):  Ashok Kumar, University of Louisiana at Lafayette

B6P-W.1  All-CMOS High-Speed CML Gates with Active Shunt-Peaking
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B6P-W.2  The Wide Input Range Automatic-Threshold Control Circuit for High Definition Digital Audio Interface
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B6P-W.3  Process Variation Compensation of a 2.4GHz LNA in 0.18um CMOS using Digitally Switchable Capacitance
Yike Cui, Tsinghua University; Baoyong Chi, Tsinghua University; Minjie Liu, Tsinghua University; Yulei Zhang, Tsinghua University; Yongming Li, Tsinghua University; Patrick Chiang, Oregon State University; Zhihua Wang, Tsinghua University

B6P-W.4  A Fully Integrated 2.4GHz CMOS Frequency Synthesizer using a Ring-Based VCO with Inductive Peaking
Ahmed Saad Abdou, LSI Logic; Khaled M. Sharaf, Ain Shams University

B6P-W.5  Fault Tolerant Signal Processing for Masking Transient Errors in VLSI Signal Processors
W.K. Jenkins, Pennsylvania State University; C. Radhakrishnan, Pennsylvania State University; S. Pal, Pennsylvania State University